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THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Confirmation No. 6157**
Masaaki YAMAUCHI et al.	:	Attorney Docket No. 2004_1445A
Serial No. 10/510,977	:	Group Art Unit 2821
Filed October 13, 2004	:	Examiner Thuy V. Tran
PLASMA DISPLAY PANEL AND METHOD OF AGING THE SAME	:	**Mail Stop AMENDMENT**

Substitute specification accepted,
Exmr. T. Tran
7/8/07

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action of December 15, 2006, please amend the above-identified application as follows.

Version with Markings to Show Changes Made

PLASMA DISPLAY PANEL AND METHOD OF AGING THE SAME

TECHNICAL FIELD

The present invention relates to an alternative current (AC) plasma display panel and a method of aging the same.

BACKGROUND ART

A plasma display panel (hereinafter referred to as a PDP or simply a panel) is a display device with an excellent visibility and a large screen, and has a low-profile and lightweight body. The difference in discharging divides PDPs into two types of the ~~alternative~~ alternating current (AC) type and the direct current (DC) type. In terms of the structure of electrodes, the PDPs fall into the 3-electrode surface discharge type and the opposing discharge type. In recent years, the dominant PDP is the AC type 3-electrode surface discharge PDP by virtue of having higher resolution and easier fabrication.

Generally, the AC type 3-electrode surface discharge PDP contains a front substrate and a back substrate disposed opposite from each other, and a plurality of discharge cells therebetween. On a front glass plate of the front substrate, scan electrodes and sustain electrodes, as display electrodes, are arranged in parallel with each other, and a dielectric layer and a protecting layer are formed over the display electrodes to cover the display electrodes. On the other hand, on a back glass plate of the back substrate, data electrodes are disposed in a parallel arrangement, and a dielectric layer is formed over the data electrodes to cover the data electrodes. On the dielectric layer between the data electrodes, a plurality of barrier ribs are formed in parallel with the rows of the data electrodes. Furthermore, a phosphor layer is formed between